

🍏 Apple Lisa Computer
Technical Information



Apple Lisa Computer:
Hardware Manual
1983
Errata (May 1985)

Lisa Computer:
1983 - 1985

Macintosh XL Hardware Information



See also: Lisa Hardware Manual (MAY 1983)

Written by: Mark Baumwell 16 May 1985

This document covers Macintosh XL information that is either incorrectly documented or not documented elsewhere.

I/O Space Addresses

The Lisa Hardware manual shows incorrect addresses for locations in the I/O space such as the expansion slots, floppy disk controller, serial ports, parallel ports, keyboard/mouse control, etc. The addresses are listed as 00xxxx in the manual, but should be FCxxxx. As an example, refer to figure 2-3 (System I/O Space Overview) in the Lisa Hardware manual. The correct addresses for the expansion slots are (all in hexadecimal):

| <u>Address</u> | <u>Function</u> |
|-----------------|-------------------------------|
| FC0000 - FC1FFF | Expansion slot #1 Low Decode |
| FC2000 - FC3FFF | Expansion slot #1 High Decode |
| FC4000 - FC5FFF | Expansion slot #2 Low Decode |
| FC6000 - FC7FFF | Expansion slot #2 High Decode |
| FC8000 - FC9FFF | Expansion slot #3 Low Decode |
| FCA000 - FCBFFF | Expansion slot #3 High Decode |

Also note that while the I/O space addresses are in the range FCxxxx, the Boot ROM addresses are in the range FExxxx. (16K Rom)

Reading the Boot ROM version number

To check the version number of the Boot ROM, display location FE3FFC for 4 bytes. If you display it from LisaBug, the display looks something like this:

00FE3FFC 0248

The version number is 0248, or 2.48. Note that 48 hex = ASCII H. Therefore, the ROM revision is H. Note the the Boot ROM version number and the Floppy ROM version number are displayed in the upper right hand corner of the Macintosh XL screen during the self test. For example if H/88 was displayed on the screen during the self test, the Boot ROM is revision H and the floppy ROM version number is 88.

Reading Parallel Interface Card ROM version numbers

Note that if a Parallel Interface Card is installed, you can check its ROM version number by adding FF8 to the start of the Low Decode address of the slot the card is in and then displaying the resulting location for 4 bytes. To interpret the version number, look at the low order byte of each word. For example, to check the ROM version number of a Parallel Interface Card in slot 2, display location FC4FF8 for 4 bytes. If you display it from LisaBug, the display looks something like this:

00FC4FF8 0001 0007

Since the ROM is on the lower half of the data bus, the upper half of the data bus should be interpreted as don't cares. Therefore, the version number is 0107, or 1.07.

Parallel Interface Card VIA offsets

Each Parallel Interface Card has two 6522 Versatile Interface Adapters (VIAs), one for each parallel port. The address of the VIAs is found by adding constants to the Expansion slot decodes as described below.

Add 2000 hex to the slot low decode to get to the lower VIA base address.

Add 2800 hex to the slot low decode to get to the upper VIA base address.

For example:

FC2000 is the slot 1 lower VIA base address.

FC2800 is the slot 1 upper VIA base address.

Internal VIA locations

There are two VIAs on the Macintosh XL I/O board. The first VIA (VIA1) is controlled by a COPS processor and is connected to the mouse, keyboard, and other peripherals. The second VIA (VIA2) controls the built-in parallel port. The VIA locations and offsets to their registers and timers are as follows:

| | | | |
|----------|------|----------|----------------------------------|
| VIA1BASE | .EQU | \$FCDD81 | ; Base address - offsets follow |
| ORB1 | .EQU | \$0 | ; Port B output Register |
| ORA1 | .EQU | \$2 | ; Port A output Register |
| DDRB1 | .EQU | \$4 | ; Port B Data Direction Register |
| DDRA1 | .EQU | \$6 | ; Port A Data Direction Register |
| T1LL1 | .EQU | \$C | ; Low Order T1 Latch |
| T1LH1 | .EQU | \$E | ; High Order T1 Latch |
| T2CL1 | .EQU | \$10 | ; Low Order T2 Counter |
| T2CH1 | .EQU | \$12 | ; High Order T2 Counter |

| | | | |
|----------|------|----------|----------------------------------|
| VIA2BASE | .EQU | \$FCD901 | ; Base address - offsets follow |
| ORB2 | .EQU | \$0 | ; Port B output Register |
| IRB2 | .EQU | \$0 | ; Port B input Register |
| ORA2 | .EQU | \$8 | ; Port A Output Register |
| IRA2 | .EQU | \$8 | ; Port A Input Register |
| DDRB2 | .EQU | \$10 | ; Port B Data Direction Register |
| DDRA2 | .EQU | \$18 | ; Port A Data Direction Register |
| T1LL2 | .EQU | \$30 | ; Low Order T1 Latch |
| T1LH2 | .EQU | \$38 | ; High Order T1 Latch |
| T2CL2 | .EQU | \$40 | ; Low Order T2 Counter |
| T2CH2 | .EQU | \$48 | ; High Order T2 Counter |

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MACINTOSH XL HARWARE INFORMATION UPDATE

Uploaded to CompuServe by Gary Kato

See also: **Lisa Hardware Manual**

Written by: Mark Baumwell (Apple Computer, Inc.)

16 May 1985

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I/O Space Addresses

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| Addresses | Function |
|-----------------|-------------------------------|
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| FC2000 - FC3FFF | Expansion slot #1 High Decode |
| FC4000 - FC5FFF | Expansion slot #2 Low Decode |
| FC6000 - FC7FFF | Expansion slot #2 High Decode |
| FC8000 - FC9FFF | Expansion slot #3 Low Decode |
| FCC000 - FCBFFF | Expansion slot #3 High Decode |

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{ Actually that's Figure 2-5. - gary - }

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Reading Parallel Interface Card ROM Version Numbers

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```
00FC4FF8  0001 0007
```

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```

VIA1BASE      .EQU    $FCDD81      ;Base address - offsets follow
ORB1          .EQU    $0           ;Port B output register
ORA1          .EQU    $2           ;Port A output register
DDRB1        .EQU    $4           ;Port B Data Direction register
DDRA1        .EQU    $6           ;Port A Data Direction register
T1LL1        .EQU    $C           ;Low Order T1 Latch
T1LH1        .EQU    $E           ;High Order T1 Latch
T2CL1        .EQU    $10          ;Low Order T2 Counter
T2CH1        .EQU    $12          ;Low Order T2 Counter

VIA2BASE      .EQU    $PCD901      ;Base address - offsets follow
ORB2          .EQU    $0           ;Port B output register
IRB2          .EQU    $0           ;Port B input register
ORA2          .EQU    $8           ;Port A output register
IRA2          .EQU    $8           ;Port A input register
DDRB2        .EQU    $10          ;Port B Data Direction register
DDRA2        .EQU    $18          ;Port A Data Direction register
T1LL2        .EQU    $30          ;Low Order T1 Latch
T1LH2        .EQU    $38          ;High Order T1 Latch
T2CL2        .EQU    $40          ;Low Order T2 Counter
T2CH2        .EQU    $48          ;Low Order T2 Counter
    
```

{ End of document - gary - }