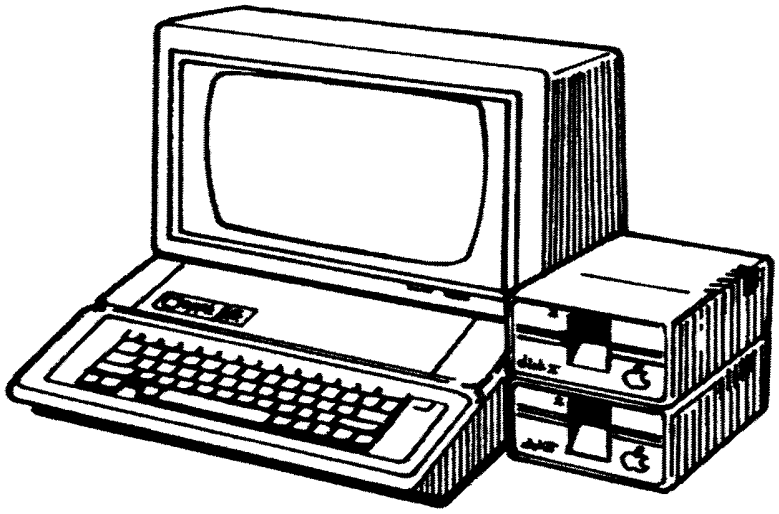
Apple ][ Computer Information

# Floppy Disk I/O Controller SWIM Chip Specification

Apple Computer, Inc. -- September 29, 1987



SOURCE
ftp://129.186.1.197/pub/netbsd/misc/wrstuden/outbox/tim/swim chip spec.pdf
31 December 2008

# SWIM CHIP SPECIFICATION

## APPLE COMPUTER, INC.

E A. B

September 29, 1987

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## INTRODUCTION

The SWIM chip is a combination of an IWM and an ISM. It should be considered as two separate chips, with minor variations.

The following document contains a description of the logic that is additional or different from the ISM and the IWM (called the Combination Logic). Attached are an ISM specification and an IWM specification. A thorough knowledge of these specifications is necessary in order to understand the signals and logic in the Combination Logic. Additional information is also found in the Swim Chip programmer's guide.

## THE COMBINATION LOGIC

### Introduction

The SWIM chip has two modes of operation, the IWM mode and the ISM mode. Only one of the modes can be active at a time. There is switching logic which selects which mode is to be used. Each mode has its own /DEV, /WRREQ, RDDATA, clock logic, etc. Unless stated otherwise, the IWM specification describes the operation of the SWIM chip in IWM mode, and the ISM specification describes the operation of the SWIM chip in the ISM mode.

### Switching Modes

The rules for switching modes are;

1) MOTOREN must be low to switch modes.
2) A mode switch from the IWM to the ISM is accomplished by four consecutive writes to the IWM mode register with Data bit 6 equal to 1, then 0, then 1, then 1.
3) A mode switch from the ISM to the IWM is accomplished by a write to the Write Zeros register with Data bit 6 equal to 1.
4) After mode switching from ISM to IWM, the very first command must be a clear L7.

5) When switching to the ISM from the IWM, the /DEV high to /DEV low timing must be no less than 4 FCLKs (if FCLK/2 is low), or 8 FCLKs (if FCLK/2 is high).

### Phase Pins

The IWM and ISM each have phase registers. Writing to either registers will change the phase outputs. There is no change due to switching modes.

The ISM has registers which control whether the Phase pins are inputs or outputs, on an individual basis. These registers are not changed by a mode switch. They now control the direction of the Phase pins in both the IWM and the ISM mode.

### Three New Bits

There are three new bits which did not exist in either the IWM or the ISM. When set (high), these bits alter the operation of the IWM. These bits can be written by a write to the CRC register ($02) with the ACTION bit low (in the ISM mode). During this write, Data bit 7 goes to the OVERRIDE bit, Data bit 6 to the M16/M8 bit, and Data bit 5 to the MODIFY bit. These bits are all cleared by /RES low. When OVERRIDE is high, it allows the combination of L4 low with a toggle of the IWM drive select (L5) to end the IWM timeout. When M16/M8 is high the IWM timer takes twice as long as normal. When MODIFY is high and ASYNC is also high, D7 will be latched as if in the PORT mode.

### A.C. and D.C. Specs

A.C. and D.C. specs and pinouts are per the ISM specification.