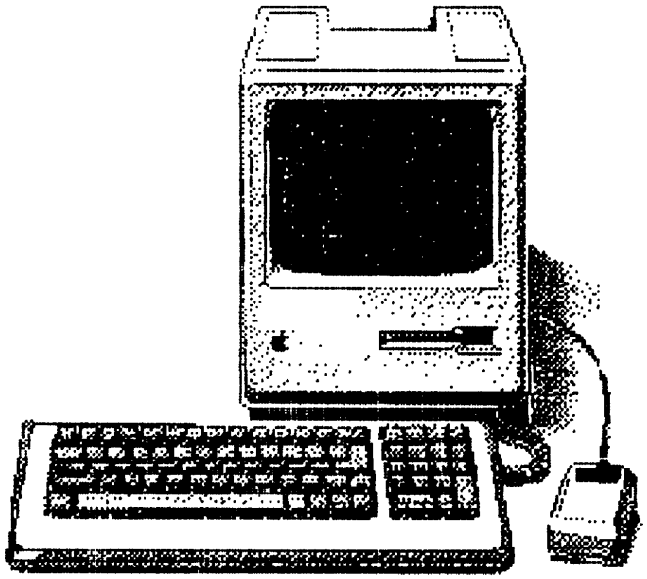
Apple Macintosh Technical Information

Macintosh Hardware Description

Macintosh Plus



28 THE MACINTOSH PLUS HARDWARE

This chapter describes the hardware features of the Macintosh Plus. Two of these features—the 800K internal disk drive and the 128K ROM—are also found in the Macintosh 512K enhanced. This chapter covers only the new features and does not repeat information already covered in chapter 2 of Volume III.

> **Note:** A partially upgraded Macintosh 512K is identical to the Macintosh 512K enhanced, while a completely upgraded Macintosh 512K includes all the features of the Macintosh Plus.

This chapter is oriented toward assembly-language programmers and assumes you're familiar with the basic operation of microprocessor-based devices. Knowledge of the Macintosh Operating System will also be helpful. To learn how your program can determine the hardware environment in which it's operating, see the description of the Environs procedure in chapter 25 of this volume.

> **Warning:** Memory sizes, addresses and other data specific to the Macintosh Plus are presented in this chapter. To maintain software compatibility across the Macintosh line, and to allow for future changes to the hardware, you're *strongly advised* to use the Toolbox and Operating System routines wherever provided. In particular, use the low-memory global variables to reference hardware; *never* use absolute addresses.

OVERVIEW OF THE HARDWARE

Features of the Macintosh 512K enhanced (not found in the Macintosh 128K and 512K) are:

- 800K internal disk drive
- 128K ROM

Features of the Macintosh Plus are:

- 800K internal disk drive
- 128K ROM
- SCSI high-speed peripheral port
- 1Mb RAM, expandable to 2Mb, 2.5Mb, or 4Mb.
- 2 Mini-8 connectors for serial ports, replacing the 2 DB-9 connectors found on the Macintosh 128K, 512K, and 512K enhanced.
- keyboard with built-in cursor keys and numeric keypad

The Macintosh Plus contains the Motorola MC68000 microprocessor clocked at 7.8336 megahertz, random access memory (RAM), read-only memory (ROM), and several chips that enable it to communicate with external devices. In addition to the five I/O devices

found in the Macintosh 128K, 512K, and 512K enhanced (the video display, sound generator, VIA, SCC and IWM), the Macintosh Plus contains a NCR 5380 Small Computer Standard Interface (SCSI) chip for high-speed parallel communication with devices such as hard disks.

In the Macintosh Plus, the 16 Mb of addressable space is divided into four equal sections. The first four megabytes are for RAM, the second four megabytes are for ROM and SCSI, the third are for the SCC, and the last four are for the IWM and the VIA. Since the devices within each block may have far fewer than four megabytes of individually addressable locations or registers, the addressing for a device may "wrap around" (a particular register appears at several different addresses) within its block.

RAM

The Macintosh Plus RAM is provided in four packages known as Single In-line Memory Modules (SIMMs). Each SIMM contains eight surface-mounted Dynamic RAM (DRAM) chips on a small printed circuit board with electrical "finger" contacts along one edge. Various RAM configurations are possible depending on whether two or four SIMMs are used and on the density of the DRAM chips that are plugged into the SIMMs:

- If the SIMMs contain 256K-bit DRAM chips, two SIMMs will provide 512K bytes of RAM, or four SIMMs will provide 1Mb of RAM (this is the standard configuration).
- If the SIMMs contain 1M-bit DRAM chips, two SIMMs will provide 2Mb of RAM, or four SIMMs will provide 4Mb of RAM.
- If two of the SIMMs contain 1M-bit DRAM chips, and two of the SIMMs contain 256K-bit DRAM chips, then these four SIMMs will provide 2.5Mb of RAM. For this configuration, the 1M-bit SIMMs must be placed in the sockets closest to the 68000 CPU.

Warning: Other configurations, such as a single SIMM or a pair of SIMMs containing DRAMs of different density, are not allowed. If only two SIMMs are installed, they must be placed in the sockets closest to the MC68000.

The SIMMs can be changed by simply releasing one and snapping in another. However, there are also two resistors on the Macintosh Plus logic board (in the area labelled "RAM SIZE") which tell the electronics how much RAM is installed. If two SIMMs are plugged in, resistor R9 (labeled "ONE ROW") must be installed; if four SIMMs are plugged in, this resistor must be removed. Resistor R8 (labelled "256K BIT") must be installed if all of the SIMMs contain 256K-bit DRAM chips. If either two or four of the SIMMs contain 1M-bit chips, resistor R8 must be removed.

Each time you turn on the Macintosh Plus, system software does a memory test and determines how much RAM is present in the machine. This information is stored in the global variable MemTop, which contains the address (plus one) of the last byte in RAM.

ROM

The Macintosh Plus contains two 512K-bit (64K x 8) ROM chips, providing 128K bytes of ROM. This is the largest size of ROM that can be installed in a Macintosh 128K, 512K, or 512K enhanced. The Macintosh Plus ROM sockets, however, can accept ROM chips of up to 1M-bit (128K x 8) in size. A configuration of two 1M-bit ROM chips would provide 256K bytes of ROM.

THE VIDEO INTERFACE

The starting addresses of the screen buffers depend on the amount of memory present in the machine. The following table shows the starting address of the main and the alternate screen buffer for various memory configurations of the Macintosh Plus:

System	Main Screen	Alternate
Macintosh Plus, 1Mb	$FA700	$F2700
Macintosh Plus, 2Mb	$1FA700	$1F2700
Macintosh Plus, 2.5Mb	$27A700	$272700
Macintosh Plus, 4Mb	$3FA700	$3F2700

Warning: To ensure that software will run on Macintoshes of different memory size, as well as on future Macintoshes, use the address stored in the global variable ScrnBase. Also, the alternate screen buffer may not be available in future versions of the Macintosh and may not be found in some software configurations of current Macintoshes.

THE SOUND GENERATOR

The starting addresses of the sound buffers depend on the amount of memory present in the machine. The following table shows the starting address of the main and the alternate sound buffer for various memory configurations of the Macintosh Plus:

System	Main Sound	Alternate
Macintosh Plus, 1Mb	$FFD00	$FA100
Macintosh Plus, 2Mb	$1FFD00	$1FA100
Macintosh Plus, 2.5Mb	$27FD00	$27A100
Macintosh Plus, 4Mb	$3FFD00	$3FA100

Warning: To ensure that software will run on Macintoshes of different memory size, as well as future Macintoshes, use the address stored in the global variable SoundBase. Also, the alternate sound buffer may not be available in future versions of the Macintosh and may not be found in some software configurations of current Macintoshes.

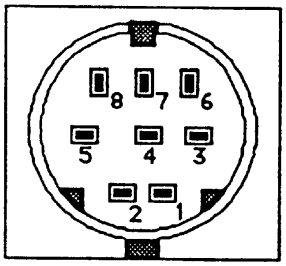
THE SCC

The Macintosh Plus uses two Mini-8 connectors for the two serial ports, replacing the two DB-9 connectors used for the serial ports on the Macintosh 128K, 512K, and 512K enhanced.

The Mini-8 connectors provide an output handshake signal, but do not provide the +5 volts and +12 volts found on the Macintosh 128K, 512K, and 512K enhanced serial ports.

The output handshake signal for each Macintosh Plus serial port originates at the SCC's Data Terminal Ready (DTR) output for that port, and is driven by an RS423 line driver. Other signals provided include input handshake/external clock, Transmit Data + and –, and Receive Data + and –.

Figure 1 shows the Mini-8 pinout for the SCC serial connectors.

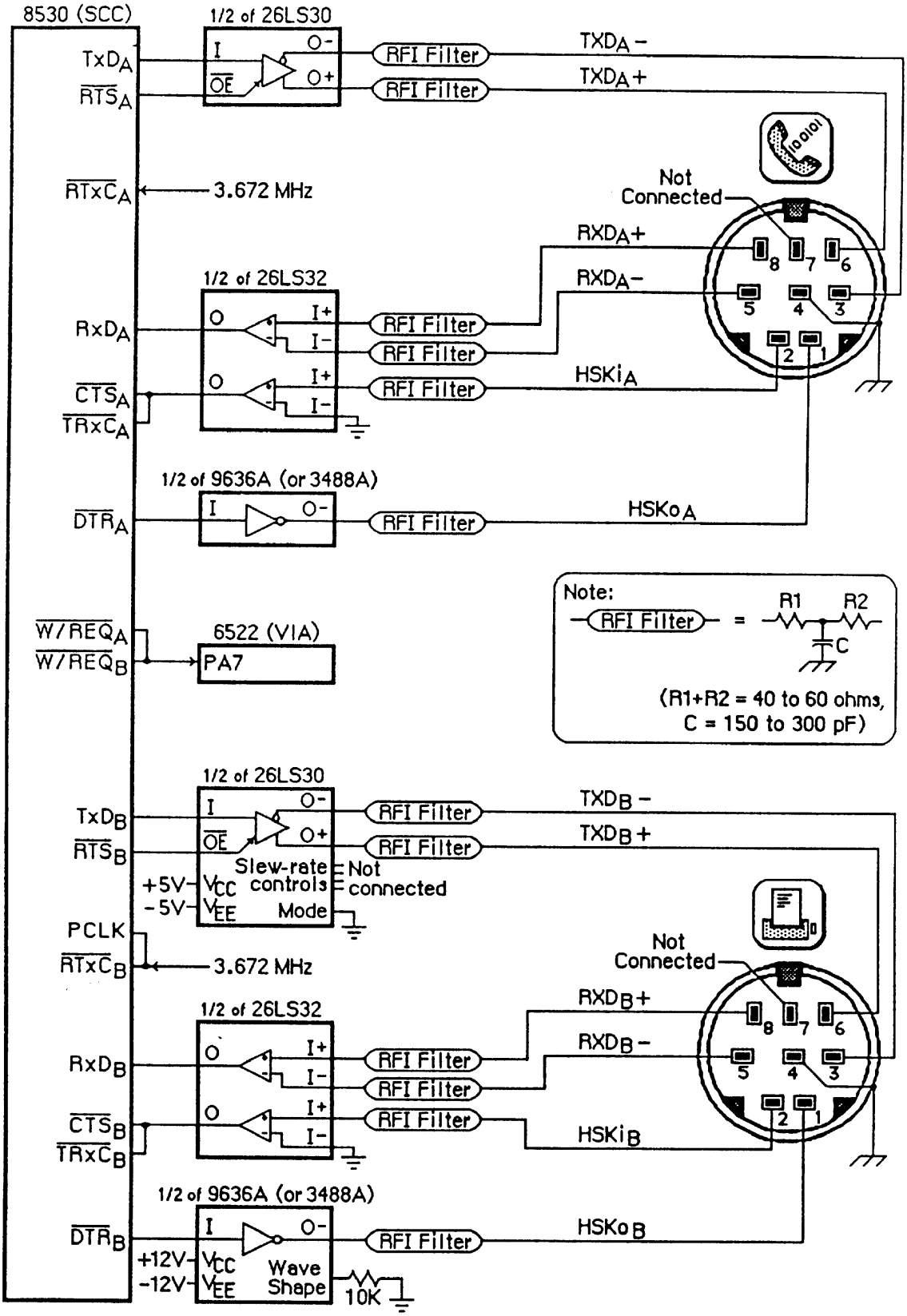


1	Output handshake
2	Input handshake / external clock
3	Transmit data –
4	Ground
5	Receive data –
6	Transmit data +
7	(not connected)
8	Receive data +

Figure 1. Pinout for SCC Serial Connectors

Diagram

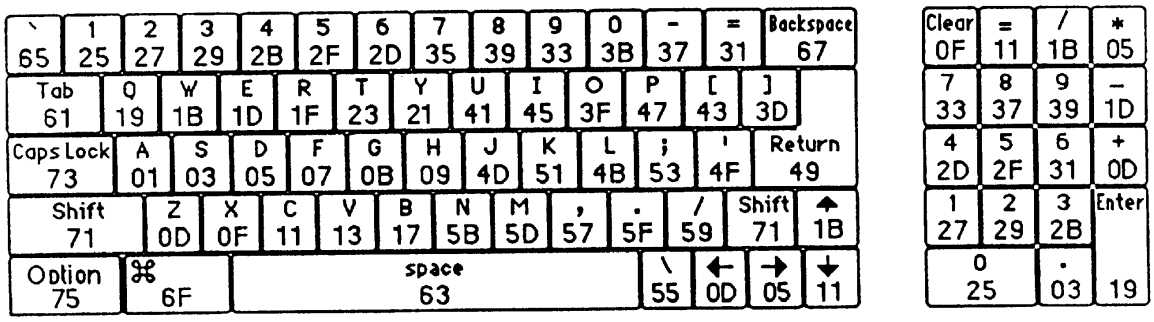
Figure 2 shows a circuit diagram for the Macintosh Plus serial ports.


8530 (SCC)
1/2 of 26LS30
TxDA
RTSA
RFI Filter
TXDA-
TXDA+
RTxCA
3.672 MHz
Not Connected
RXDA+
RXDA-
1/2 of 26LS32
RxDA
CTSA
TRxCA
HSKiA
1/2 of 9636A (or 3488A)
DTRA
HSKoA
Note:
R1
R2
C
(R1+R2 = 40 to 60 ohms, C = 150 to 300 pF)
W/REQA
W/REQB
6522 (VIA)
PA7
TxDB
RTSB
TXDB-
TXDB+
Slew-rate controls
Not connected
+5V
-5V
Mode
PCLK
RTxCB
RxDB
CTSB
TRxCB
RXDB+
RXDB-
HSKiB
DTRB
HSKoB
+12V
-12V
Wave Shape
10K

THE KEYBOARD AND KEYPAD

The Macintosh Plus keyboard, which includes a built-in numeric keypad, contains a microprocessor that scans the keys. The microprocessor contains ROM and RAM, and is programmed to conform to the same keyboard interface protocol described in chapter 2 of Volume III.

The Macintosh Plus keyboard reproduces all of the key-down transitions produced by the keyboard and optional keypad used by the Macintosh 128K, 512K, and 512K enhanced; the Macintosh Plus keyboard is also completely compatible with these other machines. If a key transition occurs for a key that used to be on the optional keypad in *lowercase*, the Macintosh Plus keyboard still responds to an Inquiry command by sending back the Keypad response ($79) to the Macintosh Plus. If a key transition occurs for an key that used to be on the optional keypad in *uppercase*, the Macintosh Plus keyboard responds to an Inquiry command by sending back the Shift Key–down Transition response ($71), followed by the Keypad response ($79). The responses for key-down transitions on the Macintosh Plus are shown (in hexadecimal) in Figure 3.



U.S. and International Keyboard

Figure 3. Key-Down Transitions

THE FLOPPY DISK INTERFACE

The Macintosh Plus has an internal double-sided disk drive; an external double-sided drive or the older single-sided drive, can be attached as well.

> **Note:** The external double-sided drive can be attached to a Macintosh 512K through the back of a Hard Disk 20. The Hard Disk 20 start-up software contains a device driver for this drive and the hierarchical (128K ROM) version of the File Manager.

The double-sided drive can format, read, and write both 800K double-sided disks and 400K single-sided disks. The operation of the drive with double-sided disks differs from that on single-sided disks. With double-sided disks, a single mechanism positions two read/write heads—one above the disk and one below—so that the drive can access two tracks simultaneously—one on the top side, and a second, directly beneath the first, on the bottom side. This lets the drive read or write two complete tracks of information before it has to move the heads, significantly reducing access time. For 400K disks, the double-sided drive restricts itself one side of the disk.

> **Warning:** Applications (for instance, copy protection schemes) should never interfere with, or depend on, disk speed control. The double-sided drive controls its own motor speed, ignoring the speed signal (PWM) from the Analog Signal Generator (ASG).

THE REAL-TIME CLOCK

The Macintosh Plus real-time clock is a new custom chip. The commands described in chapter 2 of Volume III for accessing the Macintosh 512K clock chip are also used to access the new chip. The new chip includes additional parameter RAM that's reserved by Apple. The parameter RAM information provided in chapter 13 of Volume II, as well as the descriptions of the routines used for accessing that information, apply for the new clock chip as well.

THE SCSI INTERFACE

The NCR 5380 **Small Computer Standard Interface** (SCSI) chip controls a high-speed parallel port for communicating with up to seven SCSI peripherals (such as hard disks, streaming tapes, and high speed printers). The Macintosh Plus SCSI port can be used to implement all of the protocols, arbitration, interconnections, etc. of the SCSI interface as defined by the ANSI X3T9.2 committee.

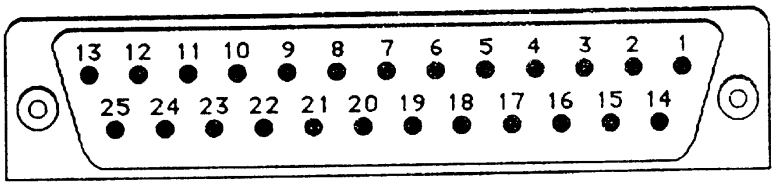
The Macintosh Plus SCSI port differs from the ANSI X3T9.2 standard in two ways. First, it uses a DB-25 connector instead of the standard 50-pin ribbon connector. An Apple adapter cable, however, can be used to convert the DB-25 connector to the standard 50-pin

connector. Second, power for termination resistors is not provided at the SCSI connector nor is a termination resistor provided in the Macintosh Plus SCSI circuitry.

> **Warning:** Do *not* connect an RS232 device to the SCSI port. The SCSI interface is designed to use standard TTL logic levels of 0 and +5 volts; RS232 devices may impose levels of –25 and +25 volts on some lines, thereby causing damage to the logic board.

The NCR 5380 interrupt signal is not connected to the processor, but the progress of a SCSI operation may be determined at any time by examining the contents of various status registers in the NCR 5380. SCSI data transfers are performed by the MC68000; pseudo-DMA mode operations can assert the NCR 5380 DMA Acknowledge (DACK) signal by reading or writing to the appropriate address (see table below). Approximate transfer rates are 142K-bytes per second for nonblind transfers and 312K-bytes per second for blind transfers.

Figure 4 shows the DB-25 pinout for the SCSI connector at the back of the Macintosh Plus.



1	$\overline{REQ}$	14	Ground
2	$\overline{MSG}$	15	$\overline{C/D}$
3	$\overline{I/O}$	16	Ground
4	$\overline{RST}$	17	$\overline{ATN}$
5	$\overline{ACK}$	18	Ground
6	$\overline{BSY}$	19	$\overline{SEL}$
7	Ground	20	$\overline{DBP}$
8	$\overline{DB0}$	21	$\overline{DB1}$
9	Ground	22	$\overline{DB2}$
10	$\overline{DB3}$	23	$\overline{DB4}$
11	$\overline{DB5}$	24	Ground
12	$\overline{DB6}$	25	(not connected)
13	$\overline{DB7}$		

Figure 4. Pinout for SCSI Connector

The locations of the NCR 5380 control and data registers are given in the following table as offsets from the constant scsiWr for write operations, or scsiRd for read operations. These base addresses are not available in global variables; instead of using absolute addresses, you should use the routines provided by the SCSI Manager (covered in chapter 31 of this volume).

Read and write operations must be made in bytes. Read operations must be to even addresses and write operations must be to odd addresses; otherwise an undefined operation will result.

The address of each register is computed as follows:

$580drn

where **r** represents the register number (from 0 through 7),
n determines whether it a read or write operation
(0 for reads, or 1 for writes), and
d determines whether the DACK signal to the NCR 5380 is asserted.
(0 for not asserted, 1 is for asserted)

Here's an example of the address expressed in binary:

0101 1000 0000 00d0 0rrr 000n

Note: Asserting the DACK signal applies only to write operations to the output data register and read operations from the input data register.

Symbolic Location	Memory Location	NCR 5380 Internal Register
scsiWr+sODR+DACKWr	$580201	Output Data Register with DACK
scsiRd+sIDR+DACKRd	$580260	Current SCSI Data with DACK
scsiWr+sODR	$580001	Output Data Register
scsiWr+sICR	$580011	Initiator Command Register
scsiWr+sMR	$580021	Mode Register
scsiWr+sTCR	$580031	Target Command Register
scsiWr+sSER	$580041	Select Enable Register
scsiWr+sDMAtx	$580051	Start DMA Send
scsiWr+sTDMArx	$580061	Start DMA Target Receive
scsiWr+sIDMArx	$580071	Start DMA Initiator Receive
scsiRd+sCDR	$580000	Current SCSI Data
scsiRd+sICR	$580010	Initiator Command Register
scsiRd+sMR	$580020	Mode Registor
scsiRd+sTCR	$580030	Target Command Register
scsiRd+sCSR	$580040	Current SCSI Bus Status
scsiRd+sBSR	$580050	Bus and Status Register
scsiRd+sIDR	$580060	Input Data Register
scsiRd+sRESET	$580070	Reset Parity/Interrupt

Note: For more information on the registers and control structure of the SCSI, consult the technical specifications for the NCR 5380 chip.

SUMMARY

Constants

```
; SCSI base addresses

scsiRd      .EQU    $580000     ;base address for read operations
scsiWr      .EQU    $580001     ;base address for write operations


; SCSI offsets for DACK

DACKRd      .EQU    $200        ;for use with sOCR and sIDR
DACKWr      .EQU    $200        ;for use with sOCR and sIDR

; SCSI offsets to NCR 5380 register

sCDR        .EQU    $00         ;Current SCSI Read Data (read)
sOCR        .EQU    $00         ;Output Data Register (write)
sICR        .EQU    $10         ;Initiator Command Register (read/write)
sMR         .EQU    $20         ;Mode Register (read/write)
sTCR        .EQU    $30         ;Target Command Register (read/write)
sCSR        .EQU    $40         ;Current SCSI Bus Status (read)
sSER        .EQU    $40         ;Select Enable Register (write)
sBSR        .EQU    $50         ;Bus & Status Register (read)
sDMAtx      .EQU    $50         ;DMA Transmit Start (write)
sIDR        .EQU    $60         ;Data input register (read)
sTDMArx     .EQU    $60         ;Start Target DMA receive (write)
sRESET      .EQU    $70         ;Reset Parity/Interrupt (read)
sIDMArx     .EQU    $70         ;Start Initiator DMA receive (write)
```

FINIS

New Technical Notes

Macintosh

Developer Support

HW 10 - Macintosh Plus Pinouts

Hardware

Revised by: MarkBaumwell — March 1986, March 1988

Written by: Mark Baumwell — January 1986

This note gives pinout descriptions for some of the Macintosh Plus ports and Macintosh Plus cables that are different than the Macintosh 128K and 512K.

Below are pinout descriptions for some Macintosh Plus ports and cables that are different than the Macintosh 128K and 512K. Note that any unconnected pins are omitted.

Macintosh Plus Port Pinouts

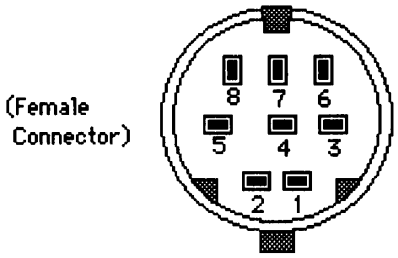


Figure 1: Macintosh Plus Serial Connectors (Mini DIN-8)

Pin	Name	Description/Notes
1	HSKo	Output Handshake (from Zilog 8530 DTR pin)
2	HSKi/External Clock	Input Handshake (CTS) or TRxC (depends on 8530 mode)
3	TxD–	Transmit Data line
4	Ground	
5	RxD–	Receive Data line
6	TxD+	Transmit Data line
7	Not connected	
8	RxD+	Receive Data line; ground this line to emulate RS232

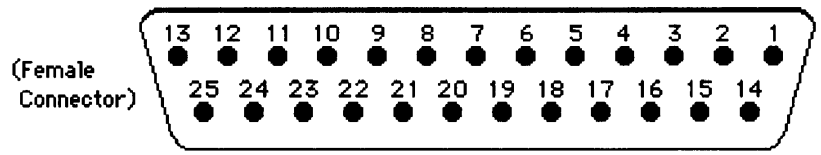


Figure 2: Macintosh Plus SCSI Connector (DB-25)

Pin	Name	Description/Notes
1	REQ–	
2	MSG–	
3	I/O–	
4	RST–	
5	ACK–	
6	BSY–	
7	Ground	
8	DB0–	
9	Ground	
10	DB3–	
11	DB5–	
12	DB6–	
13	DB7–	
14	Ground	
15	C/D–	
16	Ground	
17	ATN–	
18	Ground	
19	SEL–	
20	DBP–	
21	DB1–	
22	DB2–	
23	DB4–	
24	Ground	
25	TPWR	Not connected

Macintosh Plus Cable Pinouts

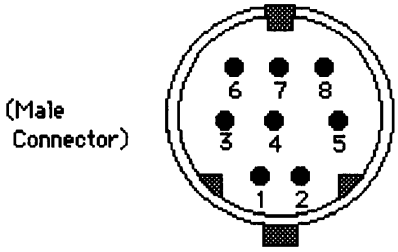


Figure 3: Apple System Peripheral-8 Cable
(connects Macintosh Plus to ImageWriter II and Apple Personal Modem)
(Product part number: M0187)
(Cable assembly part number: 590-0340-A (stamped on cable itself).

(DIN-8)	(DIN-8)
1	2
2	1
3	5
4	4
5	3
6	8
7	7
8	6

Macintosh Plus Adapter Cable
(connects Macintosh Plus DIN-8 to existing Macintosh DB-9 cables)
(Apple part number: M0189)
(Cable assembly part number: 590-0341-A (stamped on cable itself).

(DIN-8)	Name	(DB-9)	Notes
1	+12V	6	
2	HSK	7	
3	TxD–	5	
4	Ground	3	Jumpered to DB-9 pin 1 (in DB-9 connector)
5	RxD–	9	
6	TxD+	4	
7	no wire		
8	RxD+	8	
	Ground	1	Jumpered to DB-9 pin 3 (in DB-9 connector)

Further Reference:

- Macintosh Hardware Reference Manual

New Technical Notes

Macintosh

Developer Support

HW 11 - Macintosh Plus ROM Versions

Hardware

Revised by: March 1988
Written by: Cameron Birse July 1987

Readers Digest condensed version of Macintosh Plus ROM history, or the truth according to Bo3bdar the everpresent:

1st version (Lonely Hearts, checksum `4D 1E EE E1`):

Bug in the SCSI driver; won't boot if external drive is turned off. We only produced about one and a half months worth of these.

2nd version (Lonely Heifers, checksum `4D 1E EA E1`):

Fixed boot bug. This version is the vast majority of beige Macintosh Pluses.

3rd version (Loud Harmonicas, checksum 4D 1F 81 72):

Fixed bug for drives that return Unit Attention on power up or reset. Basically took the SCSI bus Reset command out of the boot sequence loop, so it will only reset once during boot sequence. This version shipped with the platinum Macintosh Pluses.

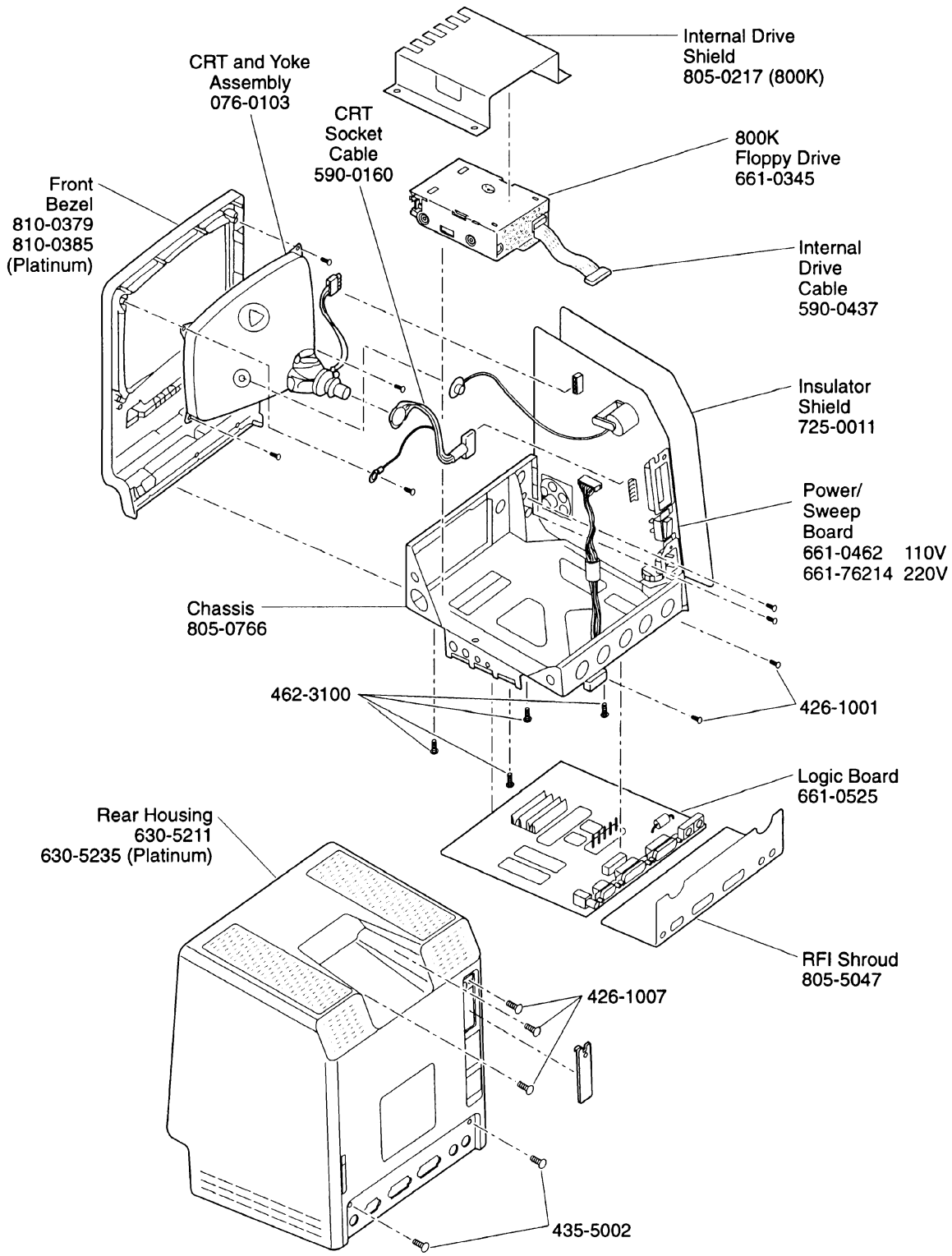
And Bo3bdar saith: "Thou shalt not rev them damn ROMs no more!"

Later that same day...

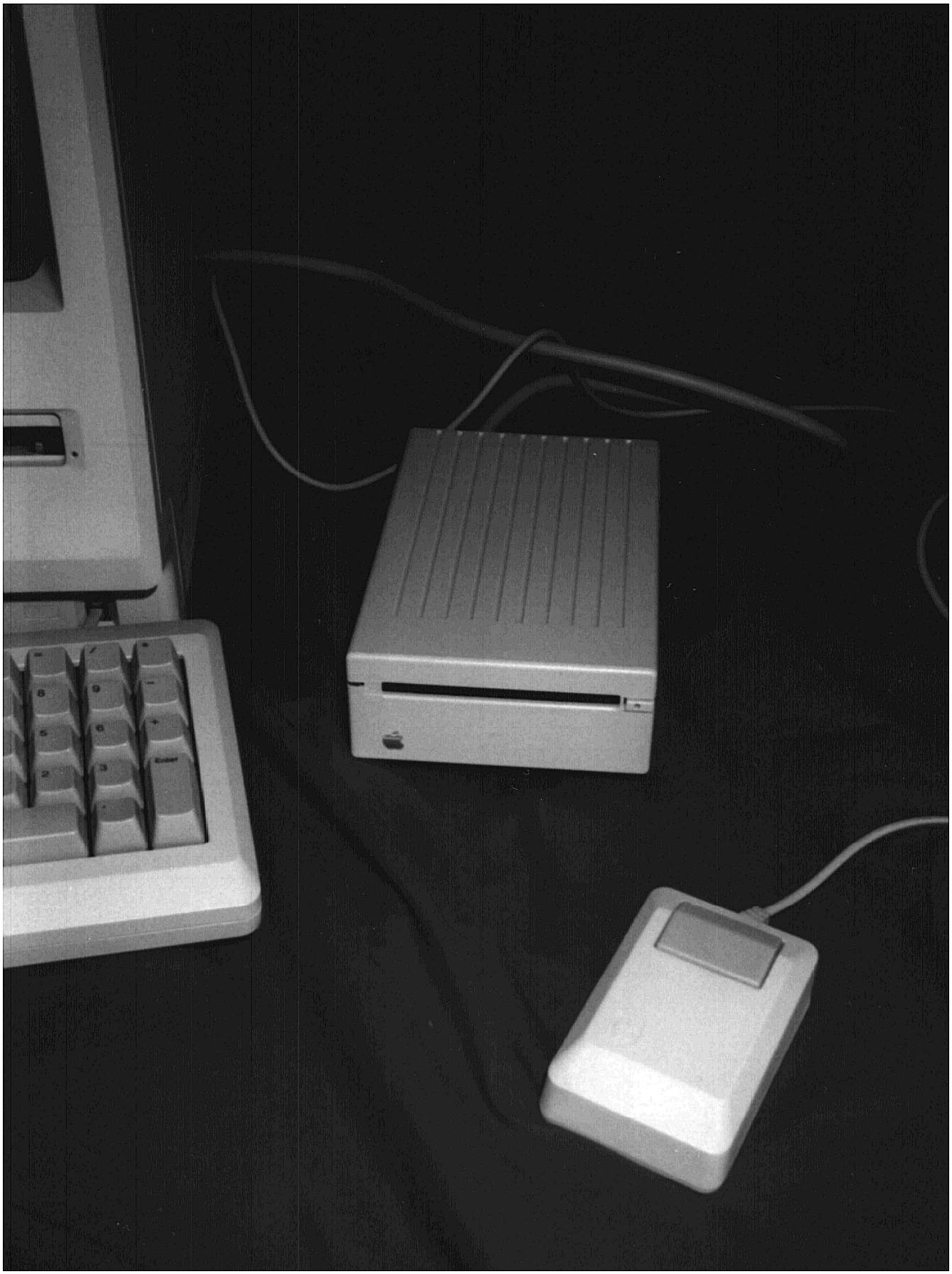
Bo3bdar Saith Also:

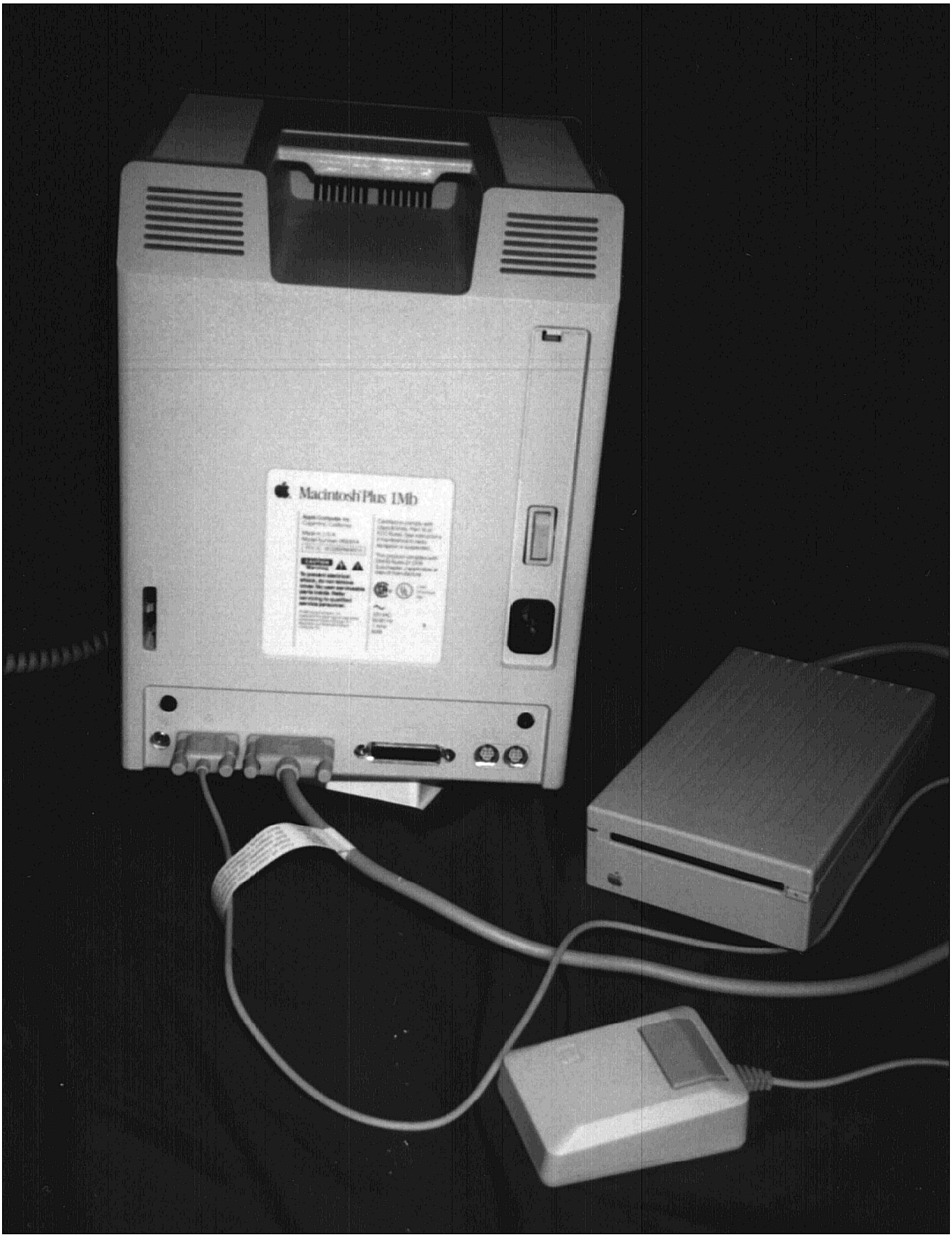
> Lonely Heifer was about a 2 byte change,
> Loud Harmonica was about 30 byte change.
> No other bug fixes in SCSI or elsewhere.
> Modified object code directly.
> Not possible to get a specific ROM since they are all the same part number.
> Shouldn't rely on a specific ROM, there will be no upgrade.
> Bo3b Bo3b a boola, a wiff Ba2m Bolom.

Exploded View Macintosh Plus

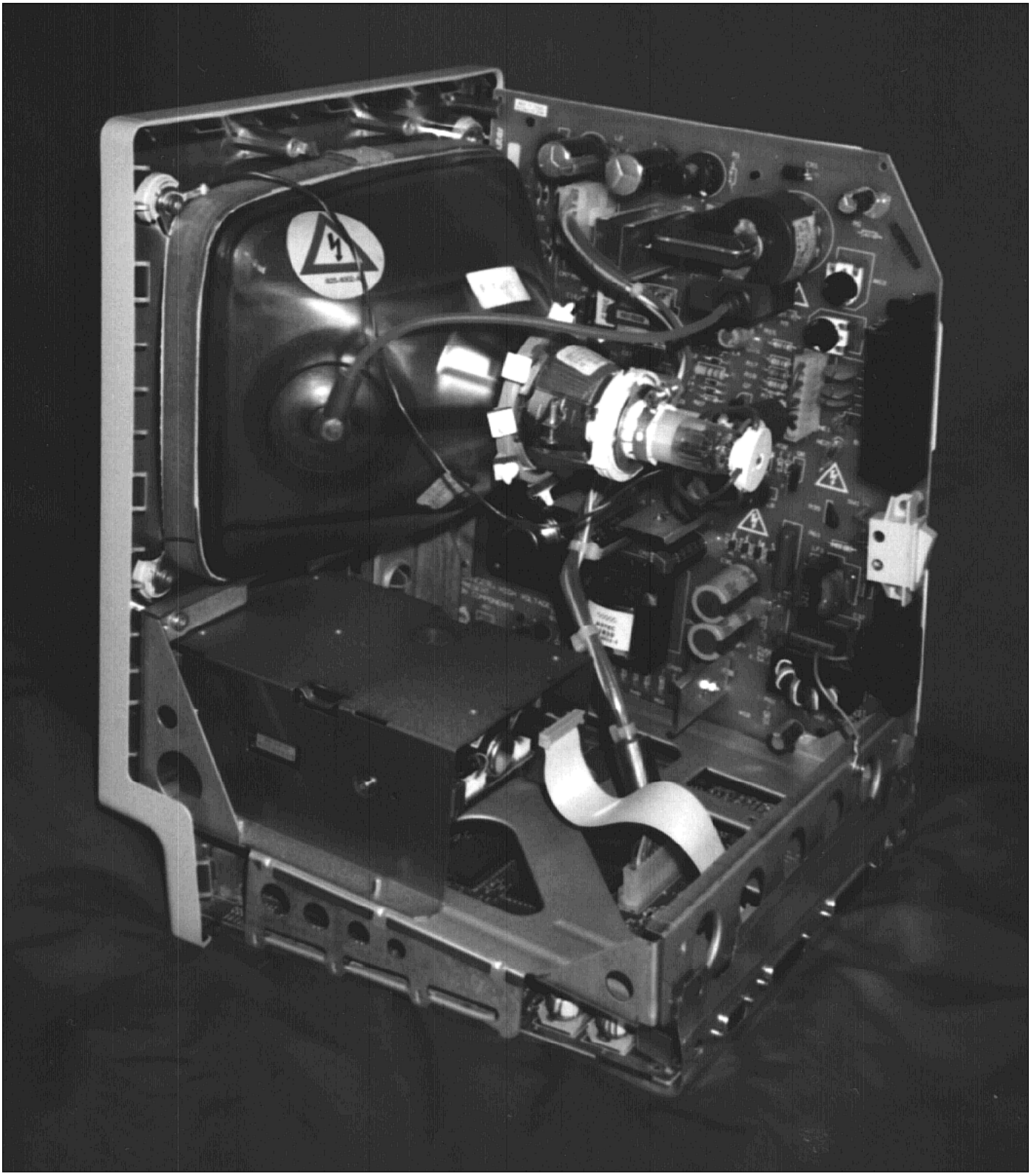


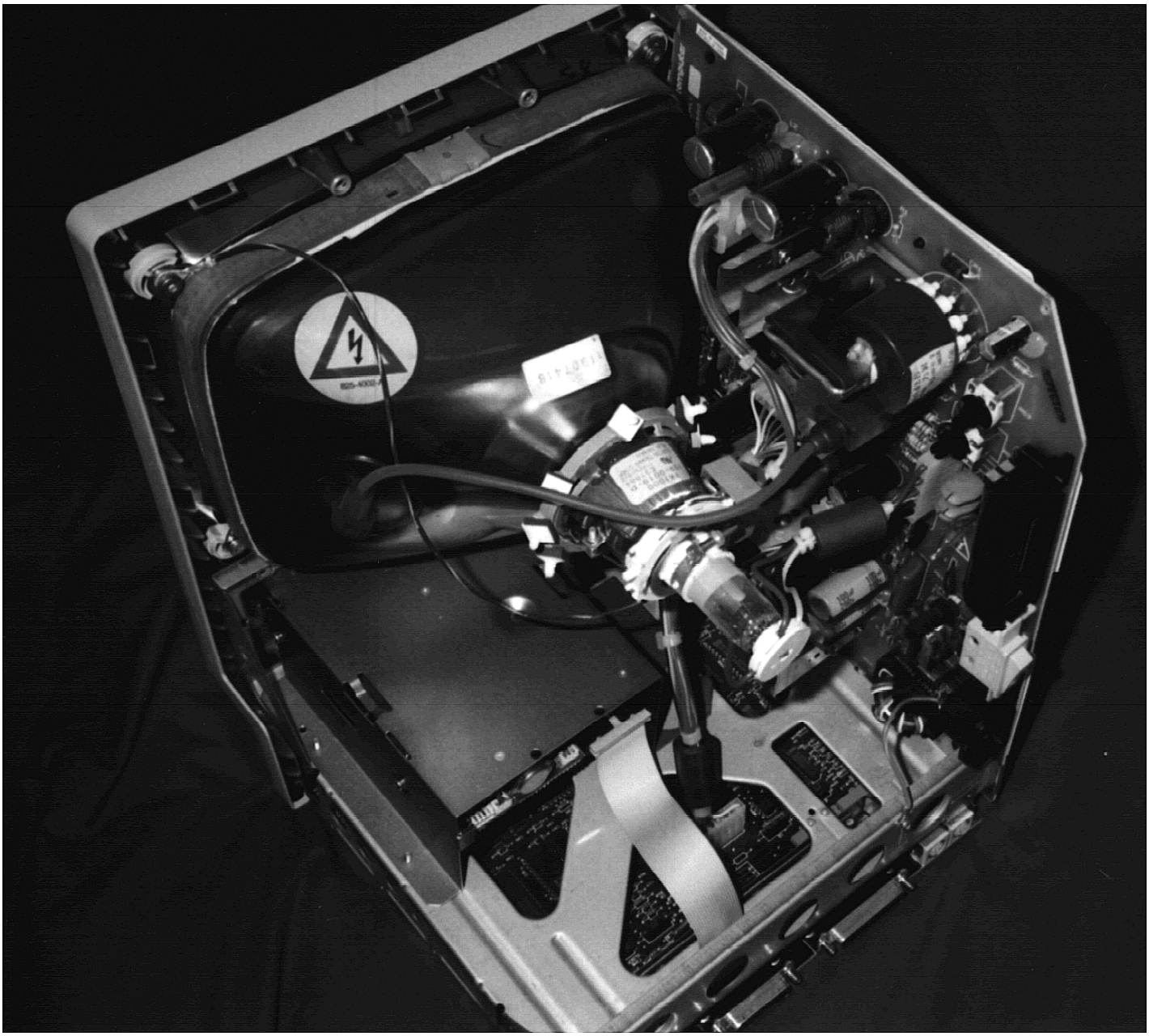

Macintosh Plus

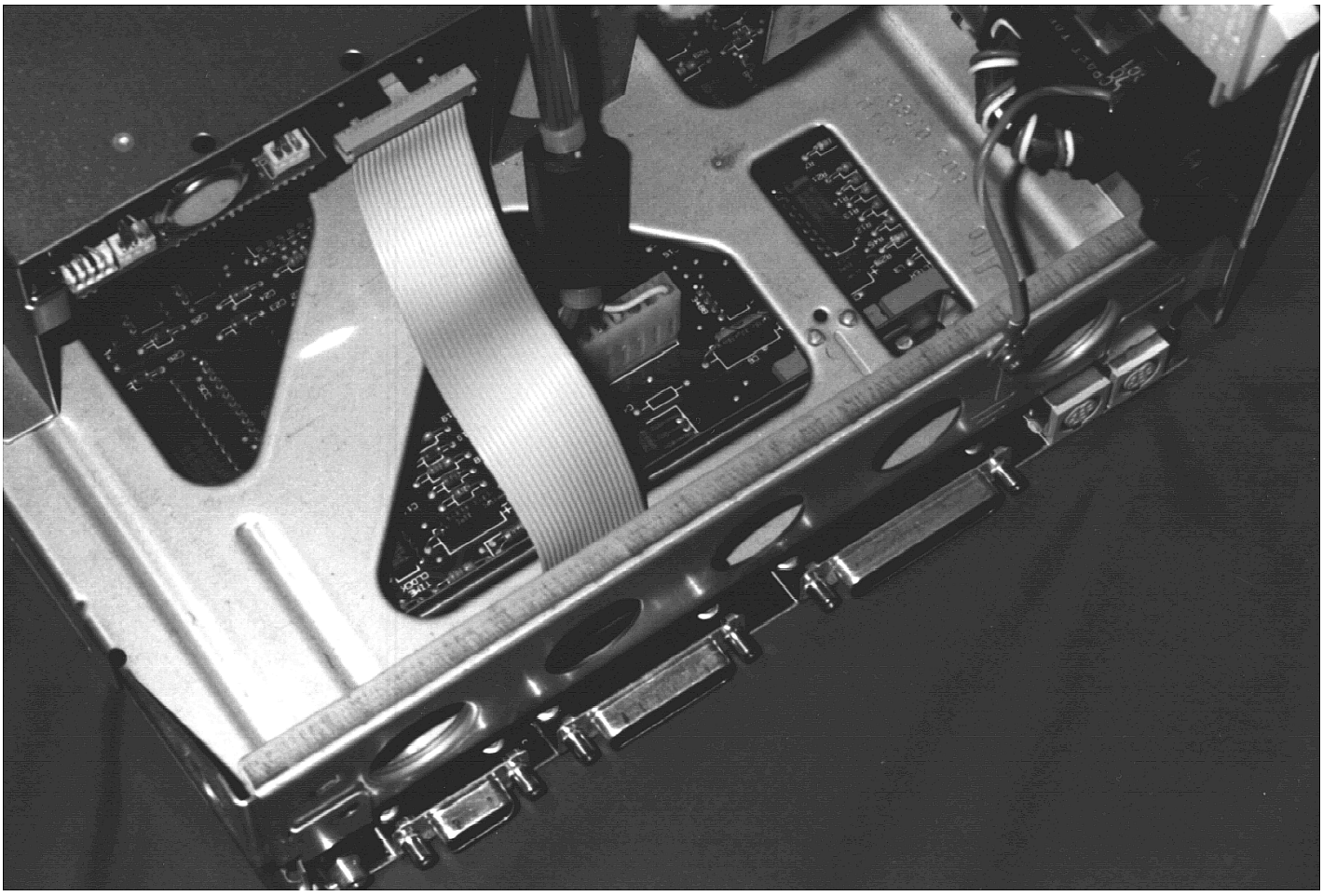


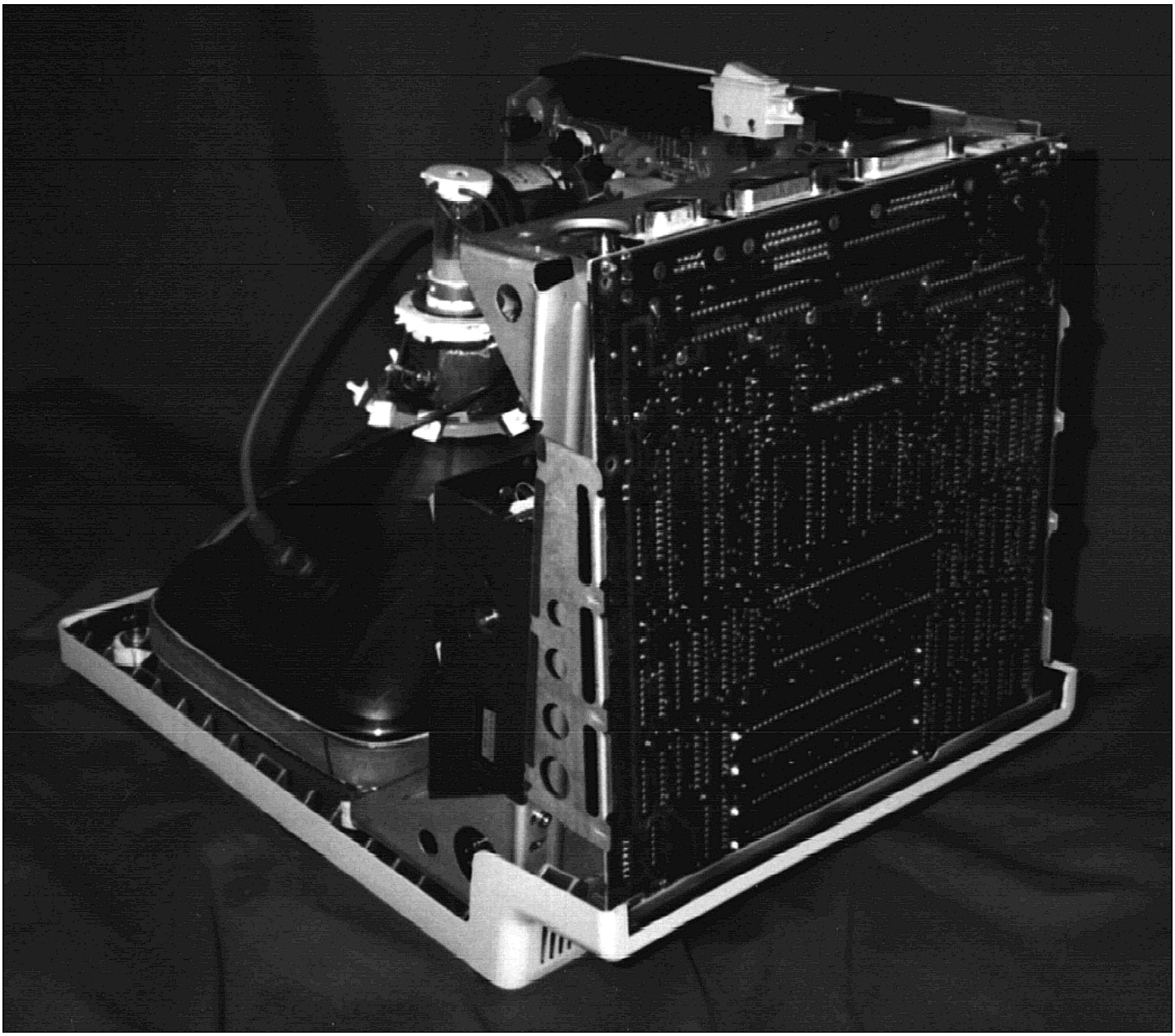

Macintosh Plus 1Mb

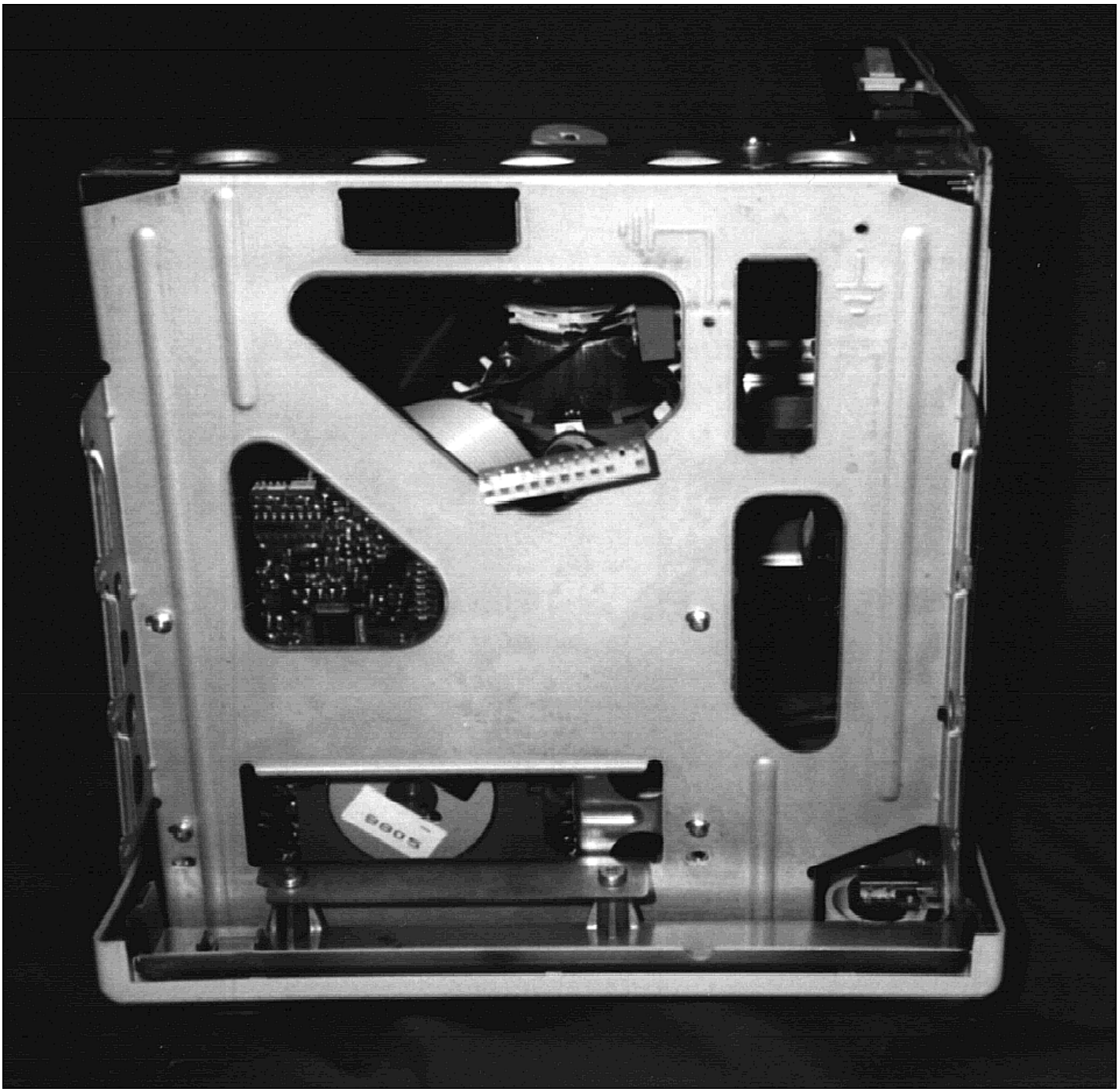

Backspace
Tab
Caps Lock
Return
Shift
Shift
Option
Clear
Enter

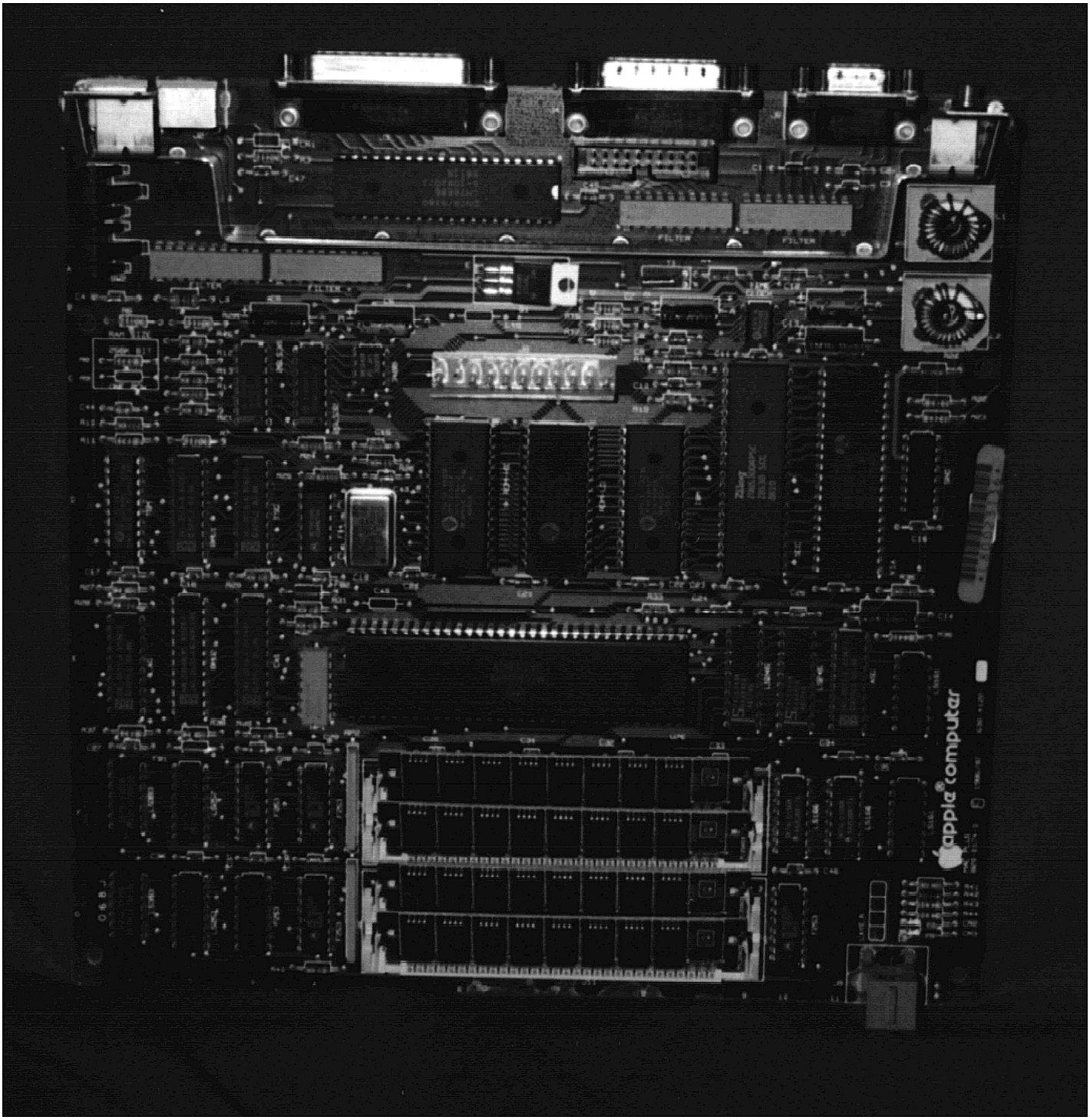








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